Exhibit D-27

DOCKET NO. SC09785TCD1

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT	Son K. Quan et al.	GROUP ART UNIT:	2831
APPLN. NO.:	09/928,737	EXAMINER:	Hung V. Ngo
FILED:	August 13, 2001	CONFIRMATION No.:	7252
TITLE:	SEMICONDUCTOR PACKAGE AND METHOD THEREFOR		

Certificate of Submission

I hereby certify that this correspondence is being submitted to the U.S.P.T.O., Alexandria, VA.

____ Addressed per C.F.R.§ 1.1(a) and deposited with the United States Postal Service with sufficient postage as first class mail.

____ Facsimile transmitted in accordance with C.F.R.§1.6(d).

XX Submitted electronically via EFS in accordance with "Legal Framework for EFS Web".

September 17, 2008
Date of Submission

/Pat Thomas/
Signature

Pat Thomas
Printed Name of Person Signing Certificate

AMENDMENT IN FURTHERANCE OF RCE UNDER 37 CFR 1.114

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants are herein filing a Request for Continued Examination under 37 CFR 1.114 of U.S. Serial No. 09/928,737 and request entrance of the following amendments in view of the remarks presented thereafter.

FEES

Applicants continue to authorize the charging of Deposit Account No. 503079 (Freescale Semiconductor, Inc.) for any fees owed in connection with this application, or credit Deposit Account No. 503079 (Freescale Semiconductor, Inc.) for any refunds.

Please amend the application as follows:

IN THE CLAIMS:

Claims 1-16 (Canceled)

17. (Currently Amended) A method for making a packaged semiconductor device comprising:

providing an interconnect substrate having a plurality of substantially identical package sites arranged in an array, the plurality of sites being separated by a singulation space;

mounting and interconnecting a semiconductor device within each site; and

overmolding a single and continuous encapsulant over each semiconductor device, the plurality of sites, and the singulation space, wherein overmolding produces a top surface of the encapsulant which has a surface deviation of less than 0.13 millimeters across a length of the encapsulant.

18. (Canceled)

19. (Canceled)

20. (Original) The method of claim 17 further comprising the step of singulating the plurality of package sites after overmolding.

21. (Original) The method of claim 20 wherein singulating comprises sawing through the single and continuous encapsulant and the interconnect substrate along the singulation space.

22. (Original) The method of claim 21 wherein singulating produces a plurality of packaged semiconductor devices, and further comprising the step of handling each packaged semiconductor device with automated pick and place equipment.

23. (New) A method for making a packaged semiconductor device comprising:

providing an interconnect substrate having a plurality of substantially identical package sites arranged in at least a four by four array, the plurality of sites being separated by a singulation space;

mounting and interconnecting a semiconductor device within each site; and

overmolding a single and continuous encapsulant over each semiconductor device, the plurality of sites, and the singulation space to produce a top surface of the encapsulant which has a surface deviation of less than 0.13 millimeters across the top surface of the encapsulant.

24. (New) The method of claim 23 further comprising the step of singulating the plurality of package sites after overmolding.

25. (New) The method of claim 24 wherein singulating comprises sawing through the single and continuous encapsulant and the interconnect substrate along the singulation space.

26. (New) The method of claim 25 wherein singulating produces a plurality of packaged semiconductor devices, and further comprising the step of handling each packaged semiconductor device with automated pick and place equipment.

27. (New) A method for making a packaged semiconductor device comprising:

providing an interconnect substrate having a plurality of substantially identical package sites arranged in an array, the plurality of sites being separated by a singulation space;

mounting and interconnecting a semiconductor device within each package site; and

overmolding an encapsulant over the plurality of sites and the singulation space to have a top surface planarity deviation of less than 0.13 millimeters.

28. (New) The method of claim 27 further comprising the step of singulating the plurality of package sites after overmolding.

29. (New) The method of claim 28 wherein singulating comprises sawing through the single and continuous encapsulant and the interconnect substrate along the singulation space.

30. (New) The method of claim 29 wherein singulating produces a plurality of packaged semiconductor devices, and further comprising the step of handling each packaged semiconductor device with automated pick and place equipment.

REMARKS

This communication is a timely response to a decision before the Board of Patent Appeals and Interferences having a notification date of July 23, 2008. No request for rehearing under 37 C.F.R. 41.52 will be filed by Applicants. The Examiner's rejection of claims 17-22 was affirmed-in-part. Under 37 C.F.R. 41.54, Applicants are timely filing a Request for Continued Examination to carry into effect the decision of the Board. Claim 17 is herein amended and claims 18 and 19 are canceled. Previously withdrawn claims 14-16 which were made the subject of an election are herein canceled to make claims 1-16 canceled. Applicants reserve the right to subsequently timely file a divisional application directed to the non-elected subject matter.

The Board's decision reversed the rejection as to claim 18. Accordingly, Applicants have herein incorporated the limitation of claim 18 into base claim 17 to place claim 17 in condition for allowance. Claim 18 is herein canceled. Applicants respectfully request the allowance of independent claim 17. In view of the amendment to base claim 17 to incorporate the subject matter of claim 18, dependent claims 19-22 are now placed in condition for allowance.

New claims 23-30 are herein added for consideration. The total number of pending claims is 12 and the total number of pending independent claims is 3. No new matter is introduced as a result of these new claims. On the basis of the Appeal Decision, independent claims 23 and 27 are allowable as each recites the feature of a "deviation of less than 0.13 millimeters" in a packaged semiconductor device having a plurality of substantially identical package sites arranged in an

array. Accordingly, Applicants respectfully request the allowance of new claims 23-30 to place the application in condition for allowance.

During the pendency of the aforementioned Appeal, information disclosure statements filed by Applicants on 04-13-04 and 07-06-05 were placed in the application file without being considered. Applicants herein request that the information in those statements be officially made of record.

Applicants thank the Examiner for the time and effort spent on the examination of this application. Applicants earnestly request the allowance of pending claims 17 and 20-30.

Respectfully submitted,

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.
Law Department
Customer Number: 23125

/Robert L. King/
Robert L. King
Reg. No.: 30,185
Phone No.: 512-996-6839
Fax No.: 512-996-6853